F50P/F50C Interface Configuration Matrix

Depending on the functions implemented with or without an onboard FPGA (i.e. I/O pins used) and front and rear I/O requirements, the following combinations are possible. The functions that can be implemented inside the FPGA depend on their respective IP core resources with regard to the FPGA capacity (33,520 LEs). Available standard configurations are highlighted in **bold blue** in the tables.

F50P

FPGA I/O pins	(No FPGA)				23	34	45	56	27	38	49	60	31	42	53	64
Front I/O	No VGA				VGA (routed to FPGA)											
	2 USB	2 USB			2 USB											
	2 ETH	2 ETH	1 ETH	-	-	1 ETH	2 ETH	-	-	1 ETH	2 ETH	-	-	1 ETH	2 ETH	-
Rear I/O		1 ETH	2 ETH	3 ETH	3 ETH	2 ETH	1 ETH	-	3 ETH	2 ETH	1 ETH	-	3 ETH	2 ETH	1 ETH	-
	2 SATA	2 SATA	2 SATA	2 SATA	2 SATA	2 SATA	2 SATA	2 SATA	1 SATA	1 SATA	1 SATA	1 SATA	-	-	-	-
	4 USB	4 USB			4 USB											
Form factor	8/12 HP	8/12 HP			12 HP											

The standard configuration is compatible with the PICMG 2.30 CompactPCI PlusIO specification.

All rear I/O Ethernet interfaces include 2 LED signals each. These could also be used for other FPGA functions instead, if no LEDs and more I/O pins are needed.

F50C

FPGA I/O pins	(No FPGA)	23	34	45	56	27	38	49	60	31	42	53	64
Front I/O	1 UART-to-USB (client) (service port)												
Rear I/O	3 ETH	3 ETH	2 ETH	1 ETH	-	3 ETH	2 ETH	1 ETH	-	3 ETH	2 ETH	1 ETH	-
	2 SATA	2 SATA	2 SATA	2 SATA	2 SATA	1 SATA	1 SATA	1 SATA	1 SATA	-	-	-	-
	4 USB												
Form factor	9 HP												

All rear I/O Ethernet interfaces include 2 LED signals each. These could also be used for other FPGA functions instead, if no LEDs and more I/O pins are needed.